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SUCCESS STORY

Applied Brain Research Tapes Out sub-50mW Processor for Edge Device AI on Synopsys Cloud

"Our vision is to set a new standard for ultra-low-power, real-time AI, powering billions of devices by enabling the optimal processing of time series data using the LMU. The LMU is a patented invention, introducing the revolutionary class of 'State Space Neural Network' models. To support us with this vision, Silicon Catalyst and Synopsys came together to provide a complete stack of EDA tools to build the world's first AI accelerator chip in record time."

– Dr. Chris Eliasmith CTO, Director, Co-Founder, Applied Brain Research

abr

Overview

Applied Brain Research, headquartered in Waterloo, Ontario, is a Silicon Catalyst Portfolio Company. Founded in 2012, ABR has developed a brain-inspired state space neural network architecture, the Legendre Memory Unit (LMU) algorithm, specifically for the challenging power and latency requirements of AI at the edge. The ABR Time Series Processor (TSP1) is a groundbreaking AI chip that natively runs LMUs and thereby offers unparalleled processing efficiency. The TSP1 provides the absolute lowest power and highest accuracy for difficult AI tasks such as real-time, full natural language transcription. https://www.appliedbrainresearch.com/

Challenges

To provide the TSP1 Edge AI hardware that achieves unparalleled processing speed with minimal power consumption, ABR had to address the following:

- **Novel architecture to natively run LMU algorithms:** Design a novel time series processor custom built to run patented LMU state space neural network models. This required best in class EDA and infrastructure resources to be able to meet power and performance numbers within a given schedule.
- **Limited resources:** Starting with a small, geographically distributed team of RandD engineers and a single EDA server, being able to scale up and work globally was critical. OPEX and CAPEX had to be kept to a minimum.
- **Failure was not an option:** First-pass working silicon providing highest efficiency and accuracy with lowest power consumption for AI at the edge applications is key to showing the value of ABR's technology. Become industry's first provider to deliver best-in-class AI hardware specifically targeted and tuned for edge applications.

> *"Industry-leading EDA tools from Synopsys, coupled with a secure and stable cloud-based platform helped us achieve unparalleled performance with the exceptional low-power operation required by edge AI applications and exceeded our expectations by delivering sub-50mW power consumption for a full vocabulary speech recognition AI application using a single chip. Using Synopsys Cloud we were able to go from our initial fabric design to full SOC implementation in one year with minimal expense and overhead."*
>
> – Kevin Conley, CEO and Director, Applied Brain Research

Solution

Backed by Silicon Catalyst, Applied Brain Research selected Synopsys as an EDA and IP partner. With Synopsys Cloud SaaS offering the entire stack of EDA and IP solutions along with a complete and robust chip design environment offering FlexEDA license management automation, unlimited infrastructure resources, built in CAD/IT support capabilities, SoC 2 Type II security compliance with seamless access to bring in PDK from leading foundries, Synopsys Cloud was the obvious choice for ABR to realize their mission.

- **EDA and IP access:** ABR leveraged the SaaS design environment to design from RTL to GDSII, along with Synopsys ARC processor IP. The Synopsys ARC Metaware Development Toolkit helped designers configure the most optimized processor configuration to integrate in design with a complete firmware stack.
- **100% utilization of engineering bandwidth:** The FlexEDA-based SaaS environment provided
  - License installation, server management, design environment, SaaS services up-time of >99%.
  - Compute cluster and shared storage was available at the click of a few buttons.
  - Managing users and access.
  - Data transfer through a secure tokenized approach.
  - Within 24-48 hour turnaround on technical issues regarding tool usage.
  - All of the above through an easy-to-use UI interface.

Bottom line, a single person equipped and managed the chip design environment with 30% less effort spent on managing on-premises environment. This allowed engineers to focus on what they do best, i.e., design chips.

> *"We leveraged a full stack of EDA tools across RTL implementation, synthesis, verification, test insertion, timing analysis, physical design and verification. In addition, we used the Synopsys ARC MetaWare Development Toolkit to integrate a configurable ARC processor, develop the ROM code, and have a complete application running on the TSP1 chip prior to tape out. The use of Synopsys Cloud infrastructure enabled our globally distributed team to do this seamlessly and to tape out a design with maximum confidence."*
>
> – Paul Lassa, Head of ASIC, Applied Brain Research

Results

Synopsys Cloud offered a one-stop-shop for complete EDA and ARC processor solutions.

- **Edge AI chip design:** Designing an AI accelerator for natively running ABR's patented LMU algorithm required careful design planning. Some of the key aspects in getting this right the first time were:
  - Low latency was a key metric, so being able to synthesize for maximum clock rates and validate performance through full system simulation was key.
  - Physical size and cost were also two critical factors and being able to achieve minimum layout size for the smallest die area was critical.
- **All in one solution:** With complete EDA and IP delivered through a SaaS platform, Synopsys provided a holistic and cost-effective approach to meet the needs of ABR and helped deliver first pass silicon in a little over 1 year.

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