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Cisco Enhances ASIC Observability and Reliability with Synopsys Silicon Lifecycle Management (SLM) IPs

Overview

With increasing transistor densities in SoC designs, maintaining reliable operation and optimizing performance and power have become more complex. Cisco's Silicon One ASICs are at the forefront of networking technology, requiring advanced monitoring to ensure they meet the highest standards of performance and dependability. To address these needs, Cisco turned to Synopsys SLM IPs to achieve deep, real-time observability and actionable insights across the silicon lifecycle.

Challenges

- Constant fluctuations in operating temperature and voltage accelerate transistor aging, leading to performance degradation
- Timing degradation is a concern, especially if timing slack on critical paths drops below safe thresholds
- On-chip process variations cause different transistors to perform inconsistently, complicating performance tuning
- Reliable, continuous monitoring of these parameters during ASIC operation is essential for ensuring long-term reliability and optimal performance

Solution

To address these challenges, Cisco integrated a suite of Synopsys Silicon Lifecycle Management (SLM) IPs across its latest ASICs. These IPs were strategically deployed to maximize observability and actionable insights throughout the silicon's operational life:

- **SLM Process, Voltage and Temperature Monitors (PVT):**
  - PVT Controller (PVTC): Acts as the central hub for collecting, managing, and reporting real-time data from all PVT sensors, supporting dynamic scaling of voltage and frequency for optimal operation
  - Process Detector (PD): Monitors on-chip process variations for performance consistency
  - Voltage Monitor (VM): Tracks real-time supply voltage fluctuations across high-density blocks
  - Distributed Temperature Sensor (DTS2) and Thermal Diode (TD): Provides granular thermal profiling and calibration for accurate temperature measurement
- **SLM Path Margin Monitor (PMM):** Enables continuous monitoring of critical timing paths for early detection of potential performance bottlenecks
- **SLM Clock Delay Monitor (CDM):** Measures SRAM access times and correlates them with datasheet specifications to validate timing integrity in high-speed domains

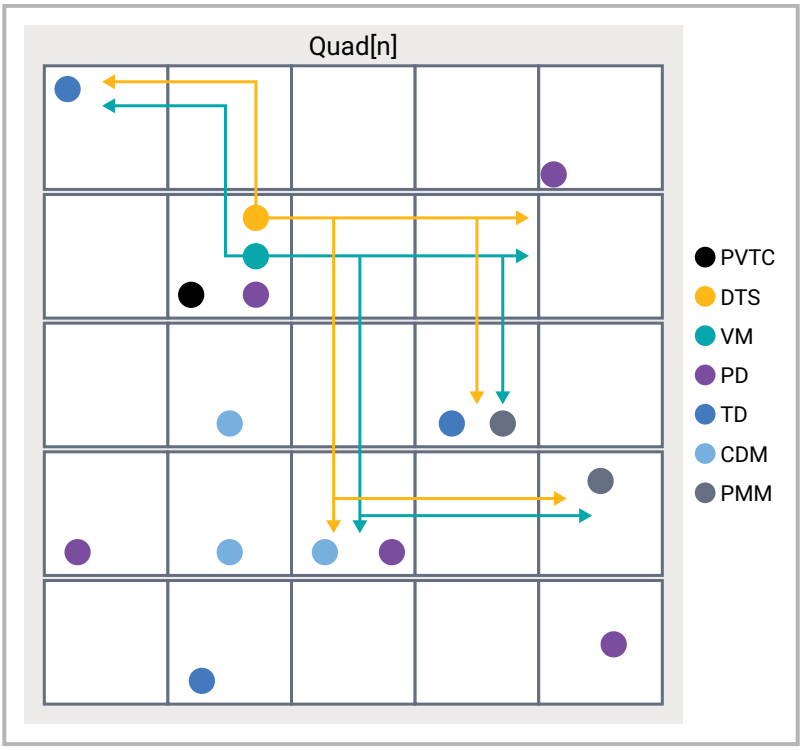

Figure 1: Placement of SLM IPs on Cisco's ASIC

Results and Benefits

- **Enhanced Real-time Observability:** The SLM IPs enabled Cisco to monitor process, voltage, and temperature parameters in real time, providing actionable data to optimize performance and power dynamically
- **Improved Reliability and Longevity:** By continuously tracking critical path margins and aging effects, Cisco can proactively manage transistor wear and extend ASIC lifespans
- **Data-Driven Design Optimization:** Insights gathered from SLM analytics are informing future design choices, helping Cisco tailor its silicon more closely to real-world operating conditions and customer requirements
- **Scalable, Application-Specific Deployment:** The modular approach allows sensor placement and count to be tailored to the unique demands of each ASIC, ensuring both efficiency and comprehensive coverage

Cisco is now focused on leveraging SLM analytics tools, including Silicon.da, to further analyze data gathered under diverse operating conditions. These insights will refine pre-silicon models for even greater power and performance optimization. By partnering with Synopsys and deploying SLM solutions, Cisco has set a new standard for ASIC observability, reliability, and performance optimization in silicon meant for advanced networking applications.

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