SYNOPSYS®

SUCCESS STORY

Synopsys and DreamBig Semiconductor

DreamBig Boosts Engineering Productivity by 20% to Tapeout AI Accelerator Chiplets with Synopsys 3DIC Compiler on Synopsys Cloud

"DreamBig's open chiplet platform, Chiplet Hub, serves the most demanding AI, datacenter, edge, storage, and automotive use cases. To achieve best in class performance and first pass silicon success for Chiplet Hub™, we leveraged the full suite of Synopsys EDA applications starting with multi-die, then front-end verification, RTL-to-GDSII implementation, extraction, timing and power analysis, and finally physical verification. We also leveraged Synopsys Verification IPs. The entire stack of EDA tools and IP was available via the Synopsys Cloud FlexEDA platform which provides fully-automated license management."

– Sohail Syed, Founder and CEO, DreamBig Semiconductor

DreamBig SEMICONDUCTOR

Overview

DreamBig, a US-based company founded in 2019 and headquartered in San Jose, CA, is an emerging semiconductor company focused on delivering comprehensive low cost, low latency, and high throughput Chiplet solutions for the AI, data center, edge compute and automotive markets. Earlier this year, DreamBig announced its Chiplet Hub™ with an industry-leading 3D HBM integration and memory-first architecture solving the most difficult challenges with scaling silicon infrastructure for AI. The 3D integrated HBM stacked on the Chiplet Hub is part of a composable memory hierarchy with SRAM, HBM, and chiplet-connected DDR, CXL memory expansion, and PCIe SSD storage. In addition, DreamBig now provides the highest-performance hardware offloaded RDMA (Remote Direct Memory Access) 800G SuperNIC solutions for open standard integration into any AI or computing platform. The DreamBig Semiconductor team is led by multi-exit veterans of the semiconductor industry, with decades of experience in ethernet networking and RDMA. Learn more at https://dreambigsemi.com/

"Using Synopsys Cloud FlexEDA licensing, we leveraged our on-premises infrastructure for running EDA workloads with complete flexibility to burst to cloud when needed. We no longer had to install and manage fixed license sets, which allowed us to focus 100% on the design at hand and tapeout our chiplet solutions several months faster than with traditional methods. FlexEDA enabled efficient license utilization and helped us maximize the EDA tool budget providing additional benefit to our valued investors."

– Steve Majors, Sr. VP of Engineering, DreamBig Semiconductor

Challenges

In order to provide low cost, low latency, and high throughput solutions, DreamBig had to address the following:

- **Open marketplace chiplet platform:** Design a disruptive open chiplet platform to be accessible to customers for horizontal innovations across the industry vs. proprietary vertical solutions from a single semiconductor supplier. This required best-in-class multi-die solution and verification protocols.
- **Design targets and standards:** Achieve low latency and high throughput while conforming to open standards so that even the most critical resources such as 3D HBM and most demanding workloads such as RDMA used in AI/DPU chiplets are plug and play. This required a full RTL-to-GDSII industry leading tool chain to meet PPA (Power, Performance and Area) constraints within schedule.
- **Critical time-to-market with first pass silicon success:** As with all startups, you only get one shot to go to market with the right technology at the right time. It must work first pass. DreamBig's teams have successfully taped out 40 designs over their careers with no silicon failures, and most of those successes have been in partnership with Synopsys.
- **Be cloud ready:** Use existing on-premises hardware resources, while being ready to scale up and leverage cloud quickly and easily.
- **CAD/IT:** Focus internal infrastructure teams on value-add automation processes that improve efficiency of the engineering organization vs. managing CAD tools and licenses.

It was important for DreamBig to address all the above challenges to make sure its chiplet based solutions for AI, data center, edge compute and automotive are ready for adoption.

Solution

DreamBig selected Synopsys' complete end-to-end EDA and IP solutions, and the Synopsys Cloud FlexEDA platform for license management.

- **Multi-die architecture:** Synopsys 3DIC Compiler facilitated early architecture exploration enabling seamless migration to 2.5/3D heterogeneous integration for the Chiplet Hub platform and chiplets that are ready to deploy on a multi-die.
- **Implementing full RTL-to-GDSII:** Synopsys Fusion Compiler was essential for meeting PPA requirements within schedule. The design flow included custom layout design using Synopsys Custom Compiler™, physical verification using Synopsys IC Validator™, parasitic extraction with Synopsys StarRC™, implementing the full RTL-to-GDSII, and finally, timing, power, and signoff checks.
- **Verification:** Synopsys VCS®, Synopsys SpyGlass®, and hardware-assisted verification using Synopsys ZeBu® EP (which supports the largest library of transactor models, memory models, and speed adaptors to run demanding workloads), and Synopsys Verification IP of industry protocols, interface, and memories (such as MIPI®, CXL, AMBA, and FLASH) were used to verify the chiplet based designs.
- **Cloud ready:** Synopsys Cloud FlexEDA enabled DreamBig to utilize its on-premises resources for chip design while automating and simplifying the task of license management. This also streamlined the move to cloud when more hardware resources were needed during the project.

> *"By bringing in Synopsys 3DIC Compiler and Fusion Compiler™ for RTL-to-GDSII implementation, we achieved industry-first 3D HBM on logic die integration while meeting all performance targets and staying within challenging power budgets to meet tight thermal constraints between logic and DRAM. Synopsys Verification IP provided the highest confidence when verifying our die-to-die interfaces for UCIe™ (Universal Chiplet Interconnect Express) and BoW (Bunch of Wires) with support for the full suite of AMBA® protocols."*

– Steve Majors, Sr. VP of Engineering, DreamBig Semiconductor

Results

Synopsys offered one-stop-shop for complete EDA and hardware-assisted verification (HAV) solutions along with flexible license management automation.

- **End-to-end chiplet design and system verification:** Starting with high-level architectural exploration, Synopsys' multi-die, verification, implementation and signoff products were key enablers of DreamBig's successful and early tapeout. In addition, Synopsys ZeBu® EP2 emulation and prototyping solutions were leveraged for post-silicon bring up readiness.
- **Time to results:**
  - Synopsys 3DIC Compiler enabled early physical architecture exploration that converged on the most efficient 3D integration of HBM stacked on logic die while balancing PPA with competing silicon resources for TSVs, macros, standard cells, and power/signal routing. The solution would have taken 6 months longer to achieve otherwise.
  - Once the system was physically architected, the partitioning of the solution into Chiplet Hub and associated chiplets required first-of-a-kind silicon implementation and trailblazing techniques. Running Fusion Compiler in-house with Synopsys support, DreamBig was able to address unique challenges and achieve on-time and on-budget tapeout.
  - Complete setup of ZeBu EP2 hardware and software including transactors was accomplished in only 3 weeks vs. 3 months planned. The use of ZeBu boosted pre-silicon verification confidence and hastened post-silicon readiness.
- **Productivity improvement:** Engineering efficiency improved by 20% due to Synopsys Cloud FlexEDA license management automation, which enabled tool license availability to match engineering demands; instead of trying to manage engineering execution within a rigid license pool.

SYNOPSYS®

©2025 Synopsys, Inc. All rights reserved. Synopsys is a trademark of Synopsys, Inc. in the United States and other countries. A list of Synopsys trademarks is available at http://www.synopsys.com/copyright.html. All other names mentioned herein are trademarks or registered trademarks of their respective owners.
07/02/25.SNPS1680712106-DreamBig-SS.